Remarks

The Office Action dated May 16, 2003, has been received and carefully noted. The amendments made herein and the following remarks are submitted as a full and complete response thereto.

As a preliminary matter, Applicants appreciate the indication of allowable subject matter in claim 6 of the present application.

Claim 1 has been amended. Applicants submit that the amendments made herein are fully supported in the specification and the drawings as originally filed, and therefore no new matter has been added. Accordingly, claims 1-6 are pending in the present application and claims 1-5 are respectfully submitted for consideration.

Claim 1 was rejected under 35 U.S.C. § 102(b) as being anticipated by Sheppard (U.S. Patent No. 4,388,705). Applicants respectfully submit that claim 1 recites subject matter that is neither disclosed nor suggested by the cited prior art.

Claim 1 recites a semiconductor device having signal lines over which signals are transferred, and a drive circuit driving the signal lines in operating modes. The operating modes including a dynamic operation mode in which the signal lines are precharged prior to transfer of the signals over said signal lines, and a static operation mode in which the signal lines are not precharged prior to transfer of the signals over said signal lines.

Accordingly, at least one of the essential features of the present invention is a dynamic operation mode in which the signal lines are precharged prior to transfer of the signals over said signal lines, and a static operation mode in which the signal lines are not precharged prior to transfer of the signals over said signal lines. As such, the

present invention results in the advantage of having a circuit for driving signals with a reduced configuration thereby reducing the chip area occupied by the circuit.

It is respectfully submitted that the prior art fails to disclose or suggest the elements of the Applicants' invention as set forth in claim 1, and therefore fails to provide the advantages which are provided by the present application.

Sheppard discloses a semiconductor memory circuit with a plurality of word lines, column lines and bit lines. A memory cell transistor of Sheppard has the gate terminal connected to the word line and the drain and source terminals connected between the bit line and the column line. A reference transistor is connected to the word line to provide a reference signal for input to a sense amplifier, and a data line is connected to the bit line to provide the data state from the data storage transistor to the sense amplifier. The data bit line and reference bit line are clamped at different pull down voltages. The memory circuit includes a reference circuit that has reference transistor which operates statically to provide a reference signal for the sense amplifier. When the word lines are being sequentially accessed the reference signal produced by the reference circuit rises to a higher average voltage and enhances the operating speed of the memory.

Applicants respectfully submit that each and every element recited within claim 1 is neither disclosed nor suggested by Sheppard. In particular, Applicants submit that the semiconductor integrated circuit device as recited in the present application is clearly distinct from that which is illustrated by the cited prior art. Specifically, it is submitted that the cited prior art fails to disclose or suggest at least the operating modes which includes "a dynamic operation mode in which the signal lines are precharged

prior to transfer of the signals over said signal lines, and a static operation mode in which the signal lines are not precharged prior to transfer of the signals over said signal lines."

It is submitted that the claimed invention is directed to a semiconductor device that drives the signal lines in two operating modes, i.e., a dynamic operating mode in which the signal lines are precharged and a static operating mode in which the signal lines are not precharged. However, Sheppard is directed to a ROM in which data is sensed by comparing a data signal with a reference signal. When word lines are successively activated to attain high-speed reading in Sheppard, the level of data signals changes, resulting in a decreased sense margin. Additionally, Sheppard uses a reference signal that changes dynamically in response to high-speed reading of memory cells, thereby preventing the sense margin from decreasing.

Specifically, column 4, lines 65-67 of Sheppard (as noted by the Examiner), discloses that the sensing circuitry is of the type which requires no precharging. Therefore, Sheppard fails to give even the slightest consideration to an operation mode that performs precharging.

Furthermore, the Examiner asserts that the read operation of Sheppard inherently includes precharging the bit lines/data lines. Applicants respectfully disagree with the Examiner's assertion because the reading of a ROM as taught by Sheppard does not require precharging in the first place.

Accordingly, Applicants respectfully submit that Sheppard fails to disclose or suggest each and every element recited in claim 1 of the present application, and therefore is allowable.

Claims 1-5 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Furutani et al. (U.S. Patent No. 5,305,261, hereinafter "Furutani") in view of Kurtze et al. (U.S. Patent No. 5,022,004, hereinafter "Kurtze"). Furutani was cited for disclosing substantially all of the claimed elements of the present invention with the exception of showing a static operation mode in which the signal lines are not precharged. Kurtze was cited for allegedly curing this deficiency. Applicants respectfully submit that each of claims 1-5 recites subject matter that is neither disclosed nor suggested by the cited prior art.

Furutani discloses a semiconductor memory device having a load circuit which precharges the internal data transmitting lines to a predetermined potential in a test mode, and a line test circuit which determines existence and nonexistence of a defective memory cell based on the potentials of the internal data transmitting lines. In the data reading operation of Furutani, the column selecting gates become conductive while the separating transistors are in OFF state, and the potential of the internal data transmitting line changes by virtue of the discharge through one of the cross-coupled MOS transistors.

Kurtze discloses a method and apparatus for improving the performance of a digital computer by reducing the latency of read operations and increasing available write bandwidth by utilizing a subset of the address bits which are the same from one operation to the next. A faster cycle type (e.g. page mode or static column) can thereby be employed in the Dynamic Random Access Memory (DRAM) memory of Kurtze by eliminating the DRAM precharge and RAS address portions of the cycle.

Applicants respectfully submit that each and every element recited within claim 1 of the present application is neither disclosed nor suggested by Furutani and/or Kurtze, taken alone or in combination. In particular, Applicants submit that the semiconductor integrated circuit device as recited in the present application is clearly distinct from that which is illustrated by the combination of the cited prior art. Specifically, it is submitted that the cited prior art fails to disclose or suggest at least the operating modes which includes "a dynamic operation mode in which the signal lines are precharged prior to transfer of the signals over said signal lines, and a static operation mode in which the signal lines are not precharged prior to transfer of the signals over said signal lines."

As noted in the Office Action, the Examiner admits that Furutani fails to "disclose a static operation mode in which the signal lines are not precharged."

It is submitted that Kurtze merely performs a series of operations including a row access, a column access, and precharging, and thus fails to cure the deficiencies which exist in Furutani. Claim 1 as amended recites a dynamic operation mode in which the signal lines are precharged prior to transfer of the signals over said signal lines, and a static operation mode in which the signal lines are not precharged prior to transfer of the signals over said signal lines. Since Kurtz merely teaches precharging bit lines prior to transfer of data over the bit lines, Kurtz does not teach the static operation mode as claimed. Accordingly, Applicants submit that Kurtze fails to disclose or suggest at least as "a dynamic operation mode in which the signal lines are precharged prior to transfer of the signals over said signal lines, and a static operation mode in which the signal lines are not precharged prior to transfer of the signals over said signal lines" recited in claim 1 of the present application, and therefore is allowable.

Moreover, Applicants submit that the is no motivation to combine the two references. In particular, it is submitted that no renewed access is made to a row address for Kurtze (i.e., no transfer of data to bit lines) Therefore, whenever renewed row access is made (i.e., whenever the transfer of data to bit lines is made), precharging is always performed beforehand in Kurtze. As such, Applicants respectfully submit that the combination of Sheppard and Kurtze teaches away from the present invention, and there is not motivation to combine the two references.

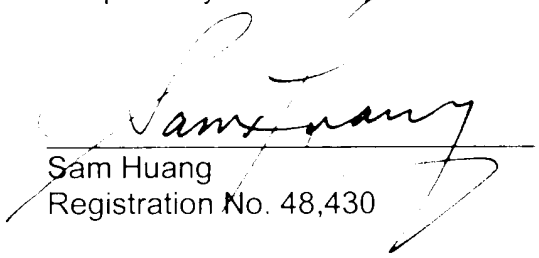
As for claims 2-5, it is submitted that each of claims 2-5 is dependent on independent claim 1. As such, each of claims 2-5 is allowable due to its dependency on allowable claim 1.

In view of the above, Applicants respectfully submit that claims 1-5, each recites subject matter that is neither disclosed nor suggested in the cited prior art. Applicants also submit that the subject matter is more than sufficient to render the claims non-obvious to a person of ordinary skill in the art, and therefore respectfully request that claims 1-5 be found allowable along with allowable claim 6, and that this application be passed to issue.

If for any reason, the Examiner determines that the application is not now in condition for allowance, it is respectfully requested that the Examiner contact the Applicants' undersigned attorney at the indicated telephone number to arrange for an interview to expedite the disposition of this application.

In the event this paper has not been timely filed, the Applicants respectfully petition for an appropriate extension of time. Any fees for such an extension, together with any additional fees that may be due with respect to this paper, may be charged to counsel's Deposit Account No. 01-2300, **referencing docket number 100353-00086**.

Respectfully submitted,



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